What is claimed is:

1. A method for providing a memory with data and write enable signals, comprising the steps of:

(A) providing the memory with a serial sequence of write enable signals;

(B) providing the memory with data that is offset in time with respect to the serial sequence of write enable signals.

2. The method of claim 1, further comprising the step of initially providing the memory with write enable signals in parallel, wherein the parallel write enable signals are for data subsequently received.

3. The method of claim 1, wherein the memory receives the serial sequence of write enable signals on a pin that can only receive write enable signals.

4. The method of claim 1, wherein the memory receives the serial sequence of write enable signals on a pin that can also send and receive data.

5. The method of claim 2, wherein the parallel write enable signals are part of a request packet.

6. The method of claim 1, wherein the memory is a dynamic random access memory (DRAM).

7. The method of claim 1, wherein there is a time gap between the time the memory is provided with the serial sequence of write enable signals and the time the memory is provided with the data that is offset in time, wherein memory operations occur during that time gap, wherein the serial

sequence of write enable signals are not applicable to the time gap memory operations.

8. A memory, comprising:

an array for data storage;

a plurality of data input pins;

a separate pin for receiving either additional data or a serial sequence of write enable signals applicable to data received by the plurality of data input pins.

9. The memory of claim 8, wherein the additional data that the separate pin can receive comprises error detection and correction (EDC) information.

10. The memory of claim 8, wherein the memory is dynamic random access memory (DRAM).

11. The memory of claim 8, wherein an external memory controller provides the memory with information as to whether the separate pin of the memory is receiving a write enable signal or receiving data.

12. The memory of claim 8, wherein each write enable signal of the serial sequence of write enable signals provides write enable information for respective data received by the data input pins at a next point in time.

13. The memory of claim 8, wherein each write enable signal of the serial sequence of write enable signals provides write enable information for respective data received by the plurality of data input pins concurrently with the write enable information received by the separate pin.

14. The memory of claim 8, wherein the plurality of data input pins can also receive write enable information.

15. The memory of claim 14, wherein each bit of the write enable information that the plurality of data input pins can receive applies to a respective subsequent unit of data received in parallel by the plurality of data input pins.

16. The memory of claim 8, wherein the separate pin for receiving either additional data or a serial sequence of write enable signals can also send data stored in the memory.

17. A method for receiving data and write enable bits for a memory, comprising the steps of:

receiving data words in parallel on a plurality of data pins; and

receiving either an additional data bit or a serial sequence of write enable bits on a separate pin, the write enable bits being applicable to the data words.

18. The method of claim 17, further comprising the step of interpreting the additional data bit as an error detection and correction (EDC) bit.

19. The method of claim 17, further comprising the step of receiving information from an external memory controller as to whether the separate pin of the memory is receiving a write enable bit or a data bit.

20. The method of claim 17, wherein the data words are received offset in time with respect to the applicable serial sequence of write enable bits.

21. The method of claim 17, wherein the data words are received concurrently with the applicable serial sequence of write enable bits.

22. The method of claim 17, further comprising the step of writing or not writing data received on the plurality of data pins as indicated by the applicable serial sequence of write enable bits.

23. The method of claim 17, further comprising the step of receiving write enable information in parallel on the plurality of data pins.

24. The method of claim 23, further comprising the step of writing or not writing data received on the plurality of data pins at a next point in time as indicated by each bit of the write enable information received in parallel on the plurality of data pins.

25. The method of claim 24, wherein there is a time gap between the time the memory receives the write enable information in parallel on the plurality of data pins and the time the memory receives the data words, wherein memory operations occur during that time gap, wherein the write enable information received in parallel on the plurality of data pins is not applicable to the time gap memory operations.

26. A memory, comprising:

an array for data storage;

a plurality of data pins for receiving either data or parallel write enable information; and

a separate pin for receiving either additional data or a serial sequence of write enable signals applicable to data received by the plurality of data input pins.

27. The memory of claim 26, wherein each write enable signal of the parallel write enable information and each write enable signal of the serial sequence of write enable signals provides write enable information for respective data received by the data pins at a next point in time.

28. The memory of claim 26, wherein the memory is dynamic random access memory (DRAM).

29. The memory of claim 26, wherein the additional data that the separate pin can receive comprises error detection and correction (EDC) information.

30. The memory of claim 29, wherein the EDC information comprises parity information relating to the data with which the parity information is received in parallel.

31. The memory of claim 29, wherein the EDC information comprises error correction code (ECC) information and wherein a plurality of bits of ECC information encode an ECC word relating to respective data received by the data pins.

32. The memory of claim 26, wherein an external memory controller provides the memory with information as to whether the separate pin of the memory is receiving a write enable signal or receiving data.

33. The memory of claim 32, wherein the information as to whether the separate pin of the memory is receiving a write enable signal or receiving data is received by a separate control pin of the memory.

34. The memory of claim 32, wherein the information as to whether the separate pin of the memory is receiving a write enable signal or receiving data is encoded by signals on a plurality of control pins of the memory.

35. The memory of claim 32, wherein the information as to whether the separate pin of the memory is receiving a write enable signal or receiving data is stored in a separate control register of the memory.

36. A method for receiving data and write enable information for a memory, comprising the steps of:

receiving either data words or write enable information in parallel on a plurality of data pins; and

receiving either an additional data bit or a serial sequence of write enable bits on a separate pin, the serial sequence of write enable bits being applicable to the data words.

37. The method of claim 36, wherein the data words are received offset in time with respect to the applicable serial sequence of write enable bits.

38. The method of claim 36, further comprising the step of writing or not writing data received on the plurality of data pins at a next point in time as indicated by the serial sequence of write enable bits and as indicated by each bit of the write enable information received in parallel on the plurality of data pins.

39. The method of claim 36, further comprising the step of interpreting the additional data bit as an error detection and correction (EDC) bit.

40. The method of claim 36, further comprising the step of receiving information from an external memory controller as to whether the separate pin of the memory is receiving a write enable bit or a data bit.

41. The method of claim 39, further comprising the step of interpreting the EDC bit as a parity bit related to the data word with which it is received in parallel.

42. The method of claim 39, further comprising the steps of:

interpreting the EDC bit as an error correction code (ECC) bit; and

interpreting a plurality of ECC bits as an ECC word encoding ECC information related to a plurality of data words.

43. The method of claim 42, further comprising the step of receiving information from an external memory controller as to whether the separate pin of the memory is receiving a write enable bit or a data bit.

44. The method of claim 43, further comprising the step of decoding the information received from the external memory controller as to whether the separate pin of the memory is receiving a write enable bit or a data bit.

45. The method of claim 43, further comprising the step of storing the information received from the external memory controller as to whether the separate pin of the memory is receiving a write enable bit or a data bit.

46. A computer system, comprising:

(A) a central processing unit (CPU) for processing data;

(B) a bus for transferring data between devices in the computer system; and

(C) a memory subsystem for storing data as directed by the CPU, the memory subsystem comprising:

(i) a dynamic random access memory (DRAM) controller for receiving directions from the CPU related to storing data and for conveying commands to a DRAM, the DRAM controller communicating with the CPU over the bus; and

(ii) a DRAM comprising:

(a) a memory array for data storage;

(b) a plurality of data pins; and

(c) a separate pin for receiving either additional data or a serial sequence of write enable signals applicable to data received by the plurality of data pins.

47. The computer system of claim 46, wherein the additional data that the separate pin can receive comprises error detection and correction (EDC) information.

48. The computer system of claim 46, wherein the DRAM controller provides the DRAM with information as to whether the separate pin of the DRAM is receiving a write enable signal or receiving data.

49. The computer system of claim 46, wherein each write enable signal of the serial sequence of write enable signals provides write enable information for respective data received by the data pins at a next point in time.

50. The computer system of claim 46, wherein each write enable signal of the serial sequence of write enable signals provides write enable information for respective data received by the plurality of data pins concurrently with the write enable information received by the separate pin.

51. The computer system of claim 46, wherein the plurality of data pins can also receive write enable information.

52. The computer system of claim 51, wherein each bit of the write enable information that the plurality of data pins can receive applies to a respective subsequent unit of data received in parallel by the plurality of data input pins.

53. The computer system of claim 51, wherein the write enable information that the plurality of data pins can receive is part of information in a DRAM request packet.